This question paper contains **4** printed pages]

Roll No. | | | | | | | | | | | |

S. No. of Question Paper : **6450**

Unique Paper Code : **251301** **D**

Name of the Paper : **Digital Electronics (ELHT-301)**

Name of the Course : **B.Sc. (H) Electronics**

Semester : **III**

Duration : **3 Hours** Maximum Marks : **75**

(Write your Roll No. on the top immediately on receipt of this question paper.)

Question number **1** is compulsory.

Attempt *five* questions in all.

Use of non-programmable scientific calculator is allowed.

1. (*a*) Covert 645.75_{10} into equivalent Binary, Octal and Hexadecimal number. 3

(*b*) Find the complement of the following function and show that $f \cdot f' = 0$, where : 3

$$f = A + CD + (A + D')(C' + D)$$

(*c*) Implement a full subtractor using 3 line to 8 line decoder. 3

(*d*) Find the characteristic equation for SR flip-flop. 3

(*e*) A memory has a capacity of 16 K × 32. Find : 3

(*i*) data input and data output lines

(*ii*) address lines

(*iii*) number of bytes.

P.T.O.

2. (*a*) Define Fan-in and Noise Margin. Explain working of positive logic CMOS NAND gate. 8

(*b*) The seven bit hamming code as received is 0010001 (MSB as P_1 and LSB as D_7). Assuming that even parity has been used, check if it is correct or not. If not, then find the correct code. 3

(*c*) Express the following functions in a sum of minterms and a product of maxterms : 4

(*i*) F(A, B, C) = (A' + B) (B' + C)

(*ii*) F(X, Y, Z) = (XY + Y'Z)

3. (*a*) Simplify the following function using Quine-Mc Cluskey method :

$$F(A, B, C, D) = \sum m\ (2, 3, 7, 10, 11, 14) + \sum d\ (1, 5, 15)$$

Also verify the result using K-map. 7

(*b*) Implement the following function using 4 × 1 MUX : 4

$$(x + y)\ (x' + z)\ (y + z')$$

(*c*) Design a combinational circuit with three inputs *x*, *y* and *z*, and three outputs A, B and C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is two less than the input. 4

4. (*a*) Draw a schematic circuit of an edge triggered JK master slave flip-flop using NAND gates. Explain its operation with the help of a truth table. 6

(*b*) The contents of a 8-bit bidirectional shift register are 11000011. What would be the contents of the register after two right shifts and then three left shifts. $D_{in} = 1$. 5

(*c*) Multiply 1101_2 by 0111_2 using the computer method. 4

5. (*a*) Design a MOD-12 asynchronous counter using JK flip-flop. 6

(*b*) Draw block diagram of four bit shift register with parallel input and serial output. 5

(*c*) Using excitation table, convert a SR flip-flop to a D flip-flop. 4

6. (*a*) Design a type T-counter that goes through states : 8

6, 3, 7, 8, 2, 9, 1, 12, 14, 0, 6, 3 .....

Also check for the bush. Give the state diagram, state table and circuit diagram.

(*b*) Show that a Johnson's counter with three flip-flops produces a sequence of six states. Also sketch its waveforms. 4

(*c*) What is a modulus of a counter ? A certain JK flip-flop has a $t_{pd} = 10$ ns. What is the largest Mod counter that can be constructed from these flip-flops and which will still operate up to 10 MHz. 3

7. (*a*) Distinguish between SRAM and DRAM. Give the internal structure of single static RAM cell using MOS transistor and explain its working. 6

(*b*) With the help of a block diagram explain the working of successive approximation ADC. 5

(*c*) The logic levels used in a 6 bit R-2R ladder DAC are 1 = 5V and 0 = 0V. What is the full scale output, percentage resolution and also find the output voltage for inputs : 4

(*i*) 010110

(*ii*) 101011